COMMENTS

The enclosed is responsive to the Examiner's Office Action mailed on December 17, 2003. Claims 1, 3-9, 13-28, 30-~~37~~ 36, ~~39~~ 39, 41-52, and 54-68 remain pending in the present application. Claims 1, 3, 4-6, 8, 15, 19, 25, 27-28, 30, 39, 52, and 54-55 have been amended. Claims 2, 10-12, 29, 37-38, 40 and 53 have been canceled. No claims have been added. The Applicants respectfully request reconsideration of the present application and the allowance of all claims.

Drawing Objections

The Examiner objected to the drawings because Figure 2b does not properly identify the two lines "SHADOWA_SEL" and "SHADOWC_SEL" outputting from Test Controller 209b. Applicants have amended Figure 2b and relocated "SHADOWA_SEL " with "SHADOWC_SEL".

The Examiner also objected to the drawings because Figure 6 604 is incorrect. The examiner believes that "SET _S/NOP" should instead read "SET _X/NOP". Figure 6 has been amended pursuant to the Examiner's suggestion.

The Applicant respectfully submits that the above-described amendments are corrections of mere matters of form and that new matter is not being added by way of these amendments. For the Examiner's convenience, a complete set of Drawings, including Replacement Sheets for Figures 2b and 6 are being submitted herewith in compliance with 37 C.F.R. § 1.85.

Disclosure Objections

The Examiner objected to the disclosure because of the following informalities: page 1 paragraph 2 refers to "core 101" twice in line 1, and also elsewhere in the specification. The examiner believes that this should recite "core 101a". Applicants have amended the Specification per the Examiner's suggestion and amended "core 101" to read "core 101a". No new matter has been added.

The disclosure is objected to because of the following informalities: page 6 paragraph 22 recites "multiplexer 214a". This multiplexer does not exist in the drawings. Applicants have amended the Specification and deleted element number 214a from paragraph [0022]. No new matter has been added.

The disclosure is objected to because of the following informalities: page 9 paragraph 32 line 2 cites "controller 209a", but the examiner believes this should recite "controller 209b". Applicants have amended the Specification per the Examiner's suggestion and amended "controller 209a" to read "controller 209b". No new matter has been added.

The disclosure is objected to because of the following informalities: page 9 paragraph 33 line 4 reads "...and WE_C for port C", but the examiner believes this should read "...and WE_C 292 for port C". Applicants have amended the

Specification per the Examiner's suggestion and amended "WE_C" to read "WE_C 292". No new matter has been added.

The disclosure is objected to because of the following informalities: page 1 0 paragraph 34 line 5 reads "SHADOWC_Sel", but the examiner believes this should read "SHADOWC_Sel 276". Applicants have amended the Specification per the Examiner's suggestion and amended "SHADOWC_Sel" for port C to read "SHADOWC_Sel 276". No new matter has been added.

The disclosure is objected to because of the following informalities: page 1 0 paragraph 35 line 5 refers to "register 297" but the examiner believes this should read "register 246". Applicants have amended the Specification per the Examiner's suggestion and amended "register 297" to read "register 246". No new matter has been added.

The disclosure is objected to because of the following informalities: page 13 paragraph 44 line 6 refers to "controller 209" but the examiner believes this should read "controller 209b". Applicants have amended the Specification per the Examiner's suggestion and amended "controller 209" to read "controller 209b". No new matter has been added.

The disclosure is objected to because of the following informalities: page 15 paragraph 50 line 4 refers to "register 245 for port A and register 246 for port B" but

the examiner believes this should read "register 244 for port A and register 245 for port B". Applicants have amended the Specification per the Examiner's suggestion and amended "register 245 for port A and register 246 for port B" to read "register 244 for port A and register 245 for port B". No new matter has been added.

The disclosure is objected to because of the following informalities: page 17 line 1 recites, "213 seen in Figure 2" but the examiner believes this should read "213 seen in Figure 2b". Applicants have amended the Specification per the Examiner's suggestion and amended "213 seen in Figure 2" to read "213 seen in Figure 2b". No new matter has been added.

The disclosure is objected to because of the following informalities: page 18 paragraph 59 line 5 refers to "combinations data" but the examiner believes this should read "combinations of data". Applicants have amended the Specification per the Examiner's suggestion and amended "combinations data" to read "combinations of data". No new matter has been added.

Claim Rejections

35 U.S.C. § 112, second paragraph, Rejections

The Examiner has concluded that claim 28 recites the limitation "said last memory", "said last memory core", "said last controller" and "said upstream controller" in lines 1-3. There is insufficient antecedent basis for this limitation in the claim. Applicants respectfully submit that claim 28 has now been amended to

depend on claim 26 rather than claim 25, and thereby providing antecedent basis for claim 28.

35 U.S.C. § 103(a) Rejections

GROUP 1

The Examiner has concluded that claims 1-3, 13-15, 17-19, and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,122,762 (hereinafter, "Ho-Ryong Kim").

Claim 1

The Applicants respectfully submit that Ho-Ryong Kim fails to teach or suggest at least the following limitations of the Applicants amended claim 1: 1) "wherein said controller further comprises an input to receive configuration commands, a first of said commands to set said controller into a transparent mode in which received test commands are ignored by said controller, a second of said commands to set said controller into a selected mode in which received test commands are executed by said controller." (Claim 1) The Examiner's attention is drawn at least to sections [0074] to [0086] of the Applicant's specification in support of the amendments made to claim 1.

Ho-Ryong Kim does not disclose that a controller can be placed into a transparent mode or a selected mode, but simply discloses an interface device that "includes a test access port (TAP) controller which operates in synchronism with a test clock signal (TCK) during test and debugging modes, and an instruction register." (Ho-Ryong Kim, col. 3, lines 36-40). Ho-Ryong Kim discloses that the

"debug controller consists of a debug control logic 410...The debug control logic 410 generates.... debug control signals in response to the memory access control signals..while in debugging mode" (Ho-Ryong Kim, col. 5, line 66 to col. 6, line 8) Therefore, at a minimum, Kim does not teach a transparency mode and a selected mode as in the Applicant's amended claim 1.

Claims 2-3, 13-15, 17-19, and 21-24

Applicants respectfully submit that independent claim 1 is allowable for reasons stated above. The Applicants respectfully submit that the dependant claims 2-3, 13-15, 17-19, and 21-24 are allowable for at least the reason that they are dependent on an allowable independent claim.

GROUP 2

The Examiner has concluded that claims 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,404,684 (hereinafter, "Arimoto") in view of U.S. Patent 5,254,942 (hereinafter, "D'Sousa"), and further in view of "Considerations for implementing IEEE 1149.1 on system-on-a-chip integrated circuits", Test Conference, 2000, Proceedings International, 3-5 Oct. 2000, pp. 628-637 (hereinafter, "Oakland").

Claims 25

The Applicants respectfully submit that the external memory test of Arimoto, the single chip IC test of D'Sousa, and the single chip considerations of Oakland fail to teach or suggest at least the following limitations of the Applicants amended claim 25: 1) "first test input to receive configuration commands sent by said test unit, a first

of said commands to set said first controller into a transparent mode in which received test commands are ignored by said first controller, a second of said commands to set said first controller into a selected mode in which received test commands are executed by said first controller" (Claim 25) The Examiner's attention is drawn at least to sections [0074] to [0086] of the Applicant's specification in support of the amendments made to claim 25.

The Applicant respectfully submits that the combination of Arimoto and D'Sousa with Oakland fails to teach or suggest a transparent mode and a selected mode. Arimoto merely discloses "a test interface circuit for allowing external direct access to the memory in a test operation mode" and "a first-in first-out circuit for successively storing data read from memory...and a control circuit for controlling data writing/reading of the first-in first-out circuit in response to an operation mode instructing signal instructing data input/output." (Arimoto, col. 7, lines 15-22) Similarly, D'Sousa teaches only a "chip that can be remotely controlled via a PC or workstation to generate stimulus and collect response data to fully test an IC which matches the footprint of the test chip." (D'Sousa Abstract) Oakland merely discloses "four issues associated with using...system-on-a-chip integrated circuits", the four issues being "simplified method for accessing debug registers", "structural information required by hardware/software development tools", "issues associated with boundary scan description language", and "high-speed boundary-scan cells that avoid a multiplexer delay." (See Oakland, Abstract) As such, neither the references nor the combination discloses a transparent mode and a selected mode.

Claims 26-28 and Claims 29-40

Applicants respectfully submit that independent claim 25 is allowable for reasons stated above. Claims 29 and claim 38 have been canceled. The Applicants respectfully submit that the dependant claims 26-28, 30-37, and 39-40 are allowable for at least the reason that they are dependent on an allowable independent claim.

GROUP 3

The Examiner has concluded that claims 41, 42 and 47-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,404,684 (hereinafter, "Arimoto"), in view of "Considerations for implementing IEEE 1149.1 on system-on-a-chip integrated circuits", Test Conference, 2000, Proceedings International, 3-5 Oct. 2000, pp. 628-637 (hereinafter, "Oakland").

Claims 41

The Applicants respectfully submit that the external memory test of Arimoto and the single chip considerations of Oakland fail to teach or suggest at least the following limitations of the Applicants' claim 41: 1) "receiving a test command at a controller; and executing said test command upon a memory core that is coupled to said controller, said test command sent from a second controller that is coupled to a second memory core, said second controller recognizing that said test command is not intended for said second controller." (Claim 41) The Examiner's attention is drawn at least to sections [0074] to [0086] of the Applicant's specification in support of claim 41.

The Applicant respectfully submits that the combination of Arimoto and Oakland fails to teach or suggest a controller that recognizes that a test command is not intended for that controller. Arimoto merely discloses "a test interface circuit for allowing external direct access to the memory in a test operation mode" and "a first-in first-out circuit for successively storing data read from memory...and a control circuit for controlling data writing/reading of the first-in first-out circuit in response to an operation mode instructing signal instructing data input/output." (Arimoto, col. 7, lines 15-22) Oakland merely discloses "four issues associated with using...system-on-a-chip integrated circuits", the four issues being "simplified method for accessing debug registers", "structural information required by hardware/software development tools", "issues associated with boundary scan description language", and "high-speed boundary-scan cells that avoid a multiplexer delay." (See Oakland, Abstract) As such, neither the references nor the combination discloses a controller that recognizes that a test command is not intended for that controller.

42 and 47-50

Applicants respectfully submit that independent claim ~~25~~ 41 is allowable for reasons stated above. The Applicants respectfully submit that the dependant claims 42 and 47-50 are allowable for at least the reason that they are dependent on an allowable independent claim.

GROUP 4

The Examiner has concluded that claims 52-56 and 61-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,254,942 (hereinafter, "D'Sousa"), in view of "Considerations for implementing IEEE 1149.1 on system-on-a-chip integrated circuits", Test Conference, 2000, Proceedings International, 3-5 Oct. 2000, pp. 628-637 (hereinafter, "Oakland")

Claim 52

The Applicants respectfully submit that the single chip IC test of D'Sousa, and the single chip considerations of Oakland fail to teach or suggest at least the following limitations of the Applicants' claim: 1) "wherein said configuration command sets said first controller to a transparent mode in which said first controller ignores subsequent test commands and forwards said subsequent configuration commands to another controller that is downstream in said daisy chain from said first controller." (Claim 52)

The Applicant respectfully submits that the combination of D'Sousa with Oakland fails to teach or suggest a transparent mode. D'Sousa teaches only a "chip that can be remotely controlled via a PC or workstation to generate stimulus and collect response data to fully test an IC which matches the footprint of the test chip." (D'Sousa Abstract) Oakland merely discloses "four issues associated with using...system-on-a-chip integrated circuits", the four issues being "simplified method for accessing debug registers", "structural information required by hardware/software development tools", "issues associated with boundary scan description language", and "high-speed boundary-scan cells that avoid a multiplexer

delay." (See Oakland, Abstract) As such, neither the references nor the combination discloses a controller having a transparent mode.

Claim 43-46, 51, 53-56, 57-60, and 61-68

Applicants respectfully submit that independent claims 41 and 52 are allowable for reasons stated above. Claim 53 has been canceled. The Applicants respectfully submit that the dependant claims 43-46, 51, 54-56, 57-60, and 61-68 are allowable for at least the reason that they are dependent on an allowable independent claim.

Invitation for a telephone interview

The Examiner is invited to call the undersigned at 408-720-8300 if there remains any issue with allowance of this case.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

Date: 3/17, 2004

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